IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicant:	Rengarajan et al.	Examiner:	Tran, T.
Serial No:	09/000,626	Group Art Unit:	2811
Filed:	December 30, 1997	Docket:	97 P 7971 US 02

For: RECESSED SHALLOW TRENCH ISOLATION STRUCTURE NITRIDE LINER AND METHOD OF MAKING SAME

Assistant Commissioner for Patents
Washington, D.C. 20231

APPELLANTS' BRIEF

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Dated: 11/2/00

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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APPEAL BRIEF

In Response to the Office Action dated April 5, 2000, finally rejecting claims 1-5, 7, 24 and 25 under 35 U.S.C. ' 112 and 35 U.S.C. ' 103, Applicants appeal pursuant to the Notice of Appeal filed on July 5, 2000 and submit this appeal brief.

1. Real Party in Interest

The real party in interest is SIEMENS CORPORATION, the assignee of the entire right title and interest in and to the subject application by virtue of an assignment recorded with the Patent Office on October 8, 1998.

2. Related Appeals and Interferences

None.

3. Status of Claims

Claims 1-5, 7, 24 and 25 are pending, stand rejected and are under appeal. A copy of the claims 1-5, 7, 24 and 25 as pending is presented in Appendix I.

4. Status of Amendments

An amendment to the claims was filed after the final rejection. These amendments were entered upon filing of the Notice of Appeal and are represented in the appendix. Claim 7 has been amended to correct a dependency error.

5. Summary of the Invention

The present invention is directed to shallow trench isolation structures employed in semiconductor memory devices. In particular, the present invention is directed to a shallow trench isolation structure for preventing hot carrier effects due to charge trapping. (Specification page 3, lines 27-30). The shallow trench isolation structure of the present invention is formed in

a trench 104 in a substrate of the memory device (See FIG. 6). An oxide liner 112 is formed lining the trench and a top surface of the substrate. A nitride liner 114 is recessed within the trench to form a recessed nitride liner 704 (FIG. 7), and the nitride liner forms a partially enclosed volume, which is completely filled with a dielectric material (material 702 in FIG. 7).

An uppermost surface of the nitride liner is disposed just below a transistor channel depth, Dc, of a transistor disposed in a well beside the shallow trench isolation structure (see FIG. 6), wherein the recessed nitride liner is dimensioned and configured to prevent hot carrier effects due to charge trapping for charge which traverses a channel of the transistor. An oxide fill (702 in FIG. 7) is disposed above the nitride liner. The oxide fill extends above and below the uppermost surface of the nitride liner substantially to a top surface of the substrate and completely filling below the uppermost surface (see FIG. 7). The oxide fill is disposed above the nitride liner such that polysilicon material used in other processing is prevented from entering the trench (specification page 8, lines 10-14).

6. Issues

1) Whether the recitation of "an uppermost surface of said nitride liner being disposed just below a transistor channel depth" in claims 1 and 24 is set forth in the specification in a way that reasonably conveys to one skilled in the relevant art that the inventors, at the time of filing, had possession of the claimed invention.

2) Whether Fukuda, Japanese Patent No. JP 57-159038 (hereinafter Fukuda), in view of Lou et al., U.S. Patent No. 5,872,045 (hereinafter Lou), Wolf, in Silicon Processing for the

VLSI Era, Vol. II, pp. 153 and 154 (hereinafter Wolf) and Hamada, U.S. Patent No. 5,972,778 (hereinafter Hamada) alone or in combination renders Applicant's claims 1 and 24 obvious.

7. Grouping of Claims

Claims 1 and 24 may be considered together. Claims 2-5 and 7 stand or fall with claim 1. Claim 25 stands or falls with claim 24.

8. Argument

A. Introduction

The present invention improves semiconductor device reliability with an improved isolation structure. The structure of the present invention includes, *inter alia*, shallow trench isolation regions, which have a nitride liner recessed below a channel depth of an adjacent transistor. By providing this recessed nitride liner, divot formation is eliminated and hot carrier trapping is reduced. Conventionally, divot formation in the shallow trench isolation structure provided the opportunity for a subsequent polysilicon deposition step to fill the divots with polysilicon. These divots filled with polysilicon caused threshold voltage reliability problems for the adjacent transistor.

The structure of the present invention sets forth, *inter alia*, an uppermost surface of said nitride liner being disposed just below a transistor channel depth, Dc, of a transistor disposed in a well beside said shallow trench isolation structure. The Examiner has rejected the specification under ' 112, first paragraph stating that the subject matter of claims 1 and 24 is not set forth in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the

time of filing, had possession of the claimed invention. The Applicant believes that this rejection is erroneous. The Applicant believes the specification provides sufficient support to reasonably convey to one skilled in the art that the Applicant had possession of the claimed invention as set forth in claims 1 and 24.

Further, as stated, the structure of the present invention sets forth, *inter alia*, an uppermost surface of said nitride liner being disposed just below a transistor channel depth, Dc, of a transistor disposed in a well beside said shallow trench isolation structure. The Examiner stated it would be obvious to modify the device of Fukuda to provide a nitride liner below a transistor depth. The Examiner has thereby rejected claims 1-5, 7, 24 and 25 as being obvious over Fukuda in view of Lou, Wolf and Hamada. The Applicants believe that the Examiner has erred since there is no disclosure or suggestion of an uppermost surface of said nitride liner being disposed just below a transistor channel depth, Dc, of a transistor disposed in a well beside the shallow trench isolation structure.

The Examiner's failure to acknowledge the afore-mentioned fundamental differences between the cited art and the presently claimed invention alone provides sufficient basis to reverse the rejection of the appealed claims. Further, the specification is believed to be enabling to one skilled in the art, as described above. Accordingly, the rejection of claims 1-5, 7, 24, and 25 should be reversed.

B. THE SPECIFICATION REASONABLY CONVEYS TO ONE SKILLED IN THE RELEVANT ART THAT THE INVENTORS, AT THE TIME OF FILING, HAD POSSESSION OF THE CLAIMED INVENTION.

The Examiner rejected to the specification under 35 CFR ' 112, first paragraph based on the recitation "an uppermost surface of said nitride liner being disposed just below a transistor channel depth" in claims 1 and 24. The Examiner stated that this recitation can be interpreted as setting forth structure not supported by the specification, and that the specification only supports the formation of an upper most surface of the nitride liner below the channel depth. The Applicant believes that the Examiner's rejection is without merit.

As long as the specification discloses at least one method [or structure] for making and using the claimed invention that bears a reasonable correlation to the entire scope of the claim, then the enablement requirement of 35 U.S.C. 112 is satisfied (brackets added). (MPEP 2164.01(b), *In re Fisher*, 427 F. 2d 833, 839, 166 USPQ 18, 24 (CCPA 1970)). "An uppermost surface of said nitride liner being disposed just below a transistor channel depth," as set forth in claims 1 and 24 is described, for example, in the present specification at page 9, lines 21 to 26, and shown in FIGS. 6 and 8. The specification clearly states that the nitride liner is below the channel depth of a transistor. The claim language " just below" is a subset of below of the channel depth. Although the Applicant believes to be entitled to broader coverage of the depth of the uppermost surface below the channel depth, the claims were previously amended to better highlight the differences between the present invention and the cited art.

One skilled in the art would understand that "below the channel depth" includes "just below the channel depth". It is therefore respectfully submitted that the Examiner erred in

rejecting the specification. Therefore, for at least these reasons, the specification is believed to be enabling and supports claims 1 and 24. Reversal of the rejection is earnestly solicited.

C. THE COMBINATION OF FUKUDA, LOU, WOLF AND HAMADA FAILS TO TEACH OR SUGGEST AN UPPERMOST SURFACE OF SAID NITRIDE LINER BEING DISPOSED JUST BELOW A TRANSISTOR CHANNEL DEPTH

Nowhere does Fukuda, Lou, Wolf and Hamada teach or suggest a shallow trench isolation structure having an uppermost surface of a nitride liner being disposed just below a transistor channel depth of a transistor disposed in a well beside said shallow trench isolation structure. At best, Fukuda shows a nitride film 4 recessed into a trench, but Fukuda fails to teach or suggest an uppermost surface of a nitride liner just below a transistor channel depth. This deficiency is not cured by the other cited references

Fukuda provides a nitride film 4 which is formed between a substrate and a SiO_2 layer and acts as a barrier to dopants to prevent an n-type inversion layer from forming where the SiO_2 contacts the substrate. This is explained on page 2 of the translation of Fukuda previously provided to the Examiner and of record. Fukuda does not disclose or suggest that the nitride film has an uppermost surface below a channel depth of a transistor disposed in a well beside the shallow trench isolation structure. In fact, Fukuda does show or suggest a transistor or any portion thereof relative to the nitride film as admitted by the Examiner. (See paper 19, page 4).

Lou fails to cure the deficiencies of Fukuda. Lou has been cited by the Examiner to teach that a trench may be filled with polysilicon as a substitute for silicon dioxide (e.g., oxide) (see paper no. 19, page 3, end of first paragraph and page 4 end of first paragraph). Lou does not

teach or suggest a nitride liner having an uppermost surface of the nitride liner being disposed just below a transistor channel depth of a transistor.

Wolf was cited by the Examiner to teach that shallow trench isolation structures may be formed 5000-8000 angstroms deep below a substrate surface (see paper no. 19, page 4), and Hamada was cited by the Examiner to teach a channel depth of 200 to 1500 angstroms deep (see paper no. 19, page 4). The Examiner stated that it is well known to form trench isolation regions below a channel depth. However, Wolf and Hamada do not teach or suggest a shallow trench isolation structure having an uppermost surface of a nitride liner being disposed just below a transistor channel depth of a transistor disposed in a well beside said shallow trench isolation structure. Rather these references merely suggest approximate depths for known structures of a semiconductor memory device.

The present invention relates to eliminating or reducing hot carrier effects, which may be caused by shallow trench isolation structures. This is provided by, *inter alia*, the shallow trench isolation structure having an uppermost surface of a nitride liner being disposed just below a transistor channel depth of a transistor disposed in a well beside said shallow trench isolation structure. The prior art references fail to teach or suggest this claimed feature. The Examiner admits that Fukuda does not disclose the uppermost surface of the nitride liner is disposed below a transistor channel depth, but maintains that this feature is obvious given the fact that isolation structures are known and that these structures are formed deeper than a channel region as supported by Wolf and Hamada. The Applicant submits that the mere fact that the prior art could be modified does not make the modification obvious unless the prior art references suggest the desirability of the modification. In re Gordan, 733 F.2d 900, 902 (Fed. Cir. 1984). In

addition, all claimed limitations must be suggested or taught by the prior art references. In re Vaeck 947 F.2d 488 (Fed. Cir. 1991).

There is no suggestion of any modification in the cited references, which would lead one skilled in art to provide the presently claimed structure. It is therefore believed that the presently claimed invention is allowable over the art of record. The cited references, alone or in combination, fail to teach or suggest the present invention. Reversal of the rejection is respectfully requested for at least the reasons stated.

Moreover, the Examiner suggests that providing a depth of the uppermost surface of the nitride liner requires only routine skill in the art. The Applicants disagree. The Examiner cites Gardener v. TEC systems, Inc. 725 F. 2d 1338, 220 USPQ 777 (Fed. Cir. 1984, cert. denied, 469 U.S. 830, 225 USPQ 232 (1984) to support his contention. In this case, the Federal Circuit held that where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and the device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device. It is respectfully submitted that Gardener does not apply in the present instance. This is due for at least the reason that the present invention performs differently from the prior art. The prior art suffers from hot carrier effects while the present invention reduces these effects thereby improving device reliability.

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981 (CCPA 1970). "All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385 (CCPA 1970). The Examiner has failed to show any

suggestion of "a shallow trench isolation structure having, *inter alia*, an uppermost surface of a nitride liner being disposed just below a transistor channel depth of a transistor disposed in a well beside the shallow trench isolation structure" in the cited prior art, and therefore has failed to establish a *prima facie* case of obviousness, since all the claimed features were not taught or suggested. The present invention is therefore believed to be allowable over the cited art.

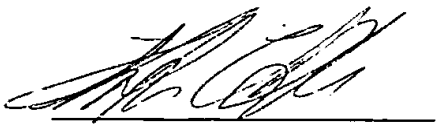
The afore-mentioned fundamental differences between the cited references and the presently claimed invention provide sufficient basis to reverse the rejection. The cited references do not, alone or in combination, teach or suggest the present invention as claimed. It is therefore asserted that the Examiner has failed to establish a *prima facie* case of obviousness. For at least these reasons, claims 1 and 24, and therefore claims 2-5, 7 and 25 are believed to be allowable. Reversal of the rejection is earnestly solicited.

D. Conclusion

The present specification is presented in a way that reasonably conveys to one skilled in the relevant art that the inventors, at the time of filing, had possession of the claimed invention. Claims 1 and 24 are therefore adequately supported. In addition, the presently invention as claimed is not disclosed or suggested by the teachings of the applied art references, either alone or in combination. Moreover, the Examiner has failed to establish a case of obviousness of the presently claimed methods under 35 U.S.C. ' 103 over Fukuda, Lou, Wolf and Hamada for at

least the reasons noted above. Accordingly, it is respectfully requested that the Board reverse the rejection of claims 1-5, 7, 24 and 25 under 35 U.S.C. ' 103.

Respectfully submitted,



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APPENDIX I: CLAIMS

1. A shallow trench isolation in a substrate, said shallow trench isolation structure comprising:

a trench in said substrate;

a nitride liner recessed within said trench and the nitride liner forming a partially enclosed volume, said partially enclosed volume being completely filled with a dielectric material which also completely fills the trench;

an uppermost surface of said nitride liner being disposed just below a transistor channel depth, Dc, of a transistor disposed in a well beside said shallow trench isolation structure, the recessed nitride liner being dimensioned and configured to prevent hot carrier effects due to charge trapping for charge which traverses a channel of the transistor;

the dielectric material including an oxide disposed above said nitride liner such that said oxide extends above the uppermost surface of said nitride liner to substantially a top surface of said substrate, such that substantially no polysilicon material is disposed within the trench.

2. A shallow trench isolation structure as recited in claim 1, wherein said transistor is a P-FET transistor.

3. A shallow trench isolation structure in a substrate as recited in claim 1, wherein the uppermost surface of said nitride liner is disposed greater than 1000 angstroms below a top surface of said substrate.

4. A shallow trench isolation structure in a substrate as recited in claim 1, further comprising:

an oxide layer disposed within the trench, said oxide layer underlying said nitride layer; and

an oxide fill disposed above said nitride liner such that the nitride liner is encapsulated by the oxide fill and oxide layer.

5. A shallow trench isolation structure in a substrate as recited in claim 4, wherein the oxide fill extends above said uppermost surface of said liner, substantially to a top surface of said substrate, such that substantially no void exists above said uppermost surface of said nitride liner.

7. A shallow trench isolation structure in a substrate as recited in claim [1] 4, wherein the oxide fill includes tetraethylortosilicate.

24. A shallow trench isolation structure for preventing hot carrier effects due to charge trapping, said shallow trench isolation structure comprising:

a trench in the substrate;

an oxide liner formed lining the trench and a top surface of the substrate;

a nitride liner recessed within said trench and the nitride liner forming a partially enclosed volume, said partially enclosed volume being completely filled with a dielectric material which also completely fills the trench;

an uppermost surface of said nitride liner being disposed just below a transistor channel depth, Dc, of a transistor disposed in a well beside said shallow trench isolation structure, the recessed nitride liner being dimensioned and configured to prevent hot carrier effects due to charge trapping for charge which traverses a channel of the transistor;

an oxide fill disposed above said nitride liner, such that said oxide fill extends above and below the uppermost surface of said nitride liner substantially to a top surface of said substrate and completely filling below the uppermost surface, respectively; and

the oxide fill is disposed above said nitride liner such that polysilicon material used in other processing is prevented from entering the trench.

25. The structure of claim 24, wherein the oxide fill includes tetraethylortosilicate.